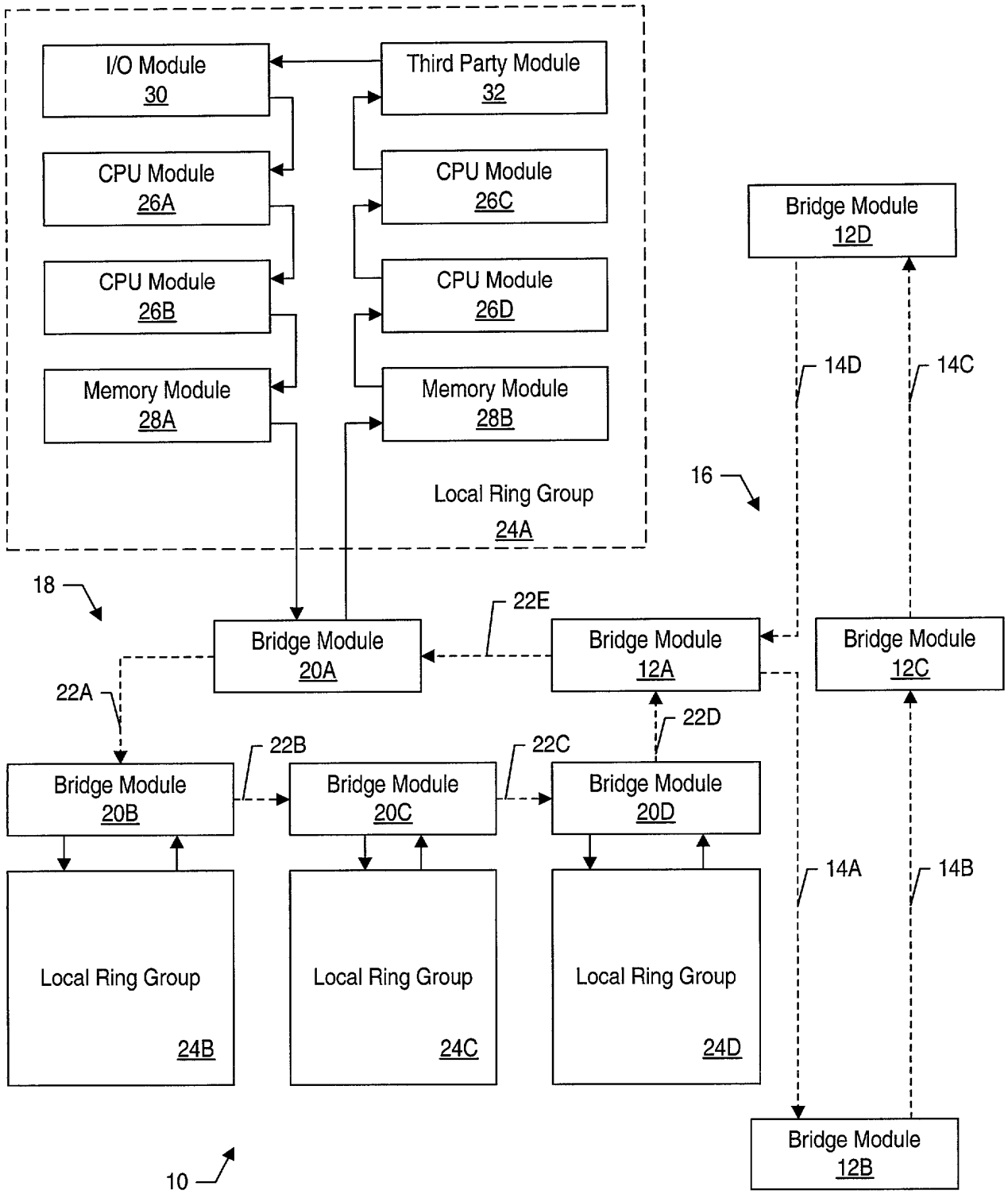
I/O Module
30
Third Party Module
32
CPU Module
26A
CPU Module
26C
CPU Module
26B
CPU Module
26D
Memory Module
28A
Memory Module
28B
Local Ring Group
24A
16
Bridge Module
12D
14D
14C
18
22E
Bridge Module
20A
Bridge Module
12A
Bridge Module
12C
22A
22D
22B
22C
Bridge Module
20B
Bridge Module
20C
Bridge Module
20D
14A
14B
Local Ring Group
24B
Local Ring Group
24C
Local Ring Group
24D
Bridge Module
12B
10

FIG. 1

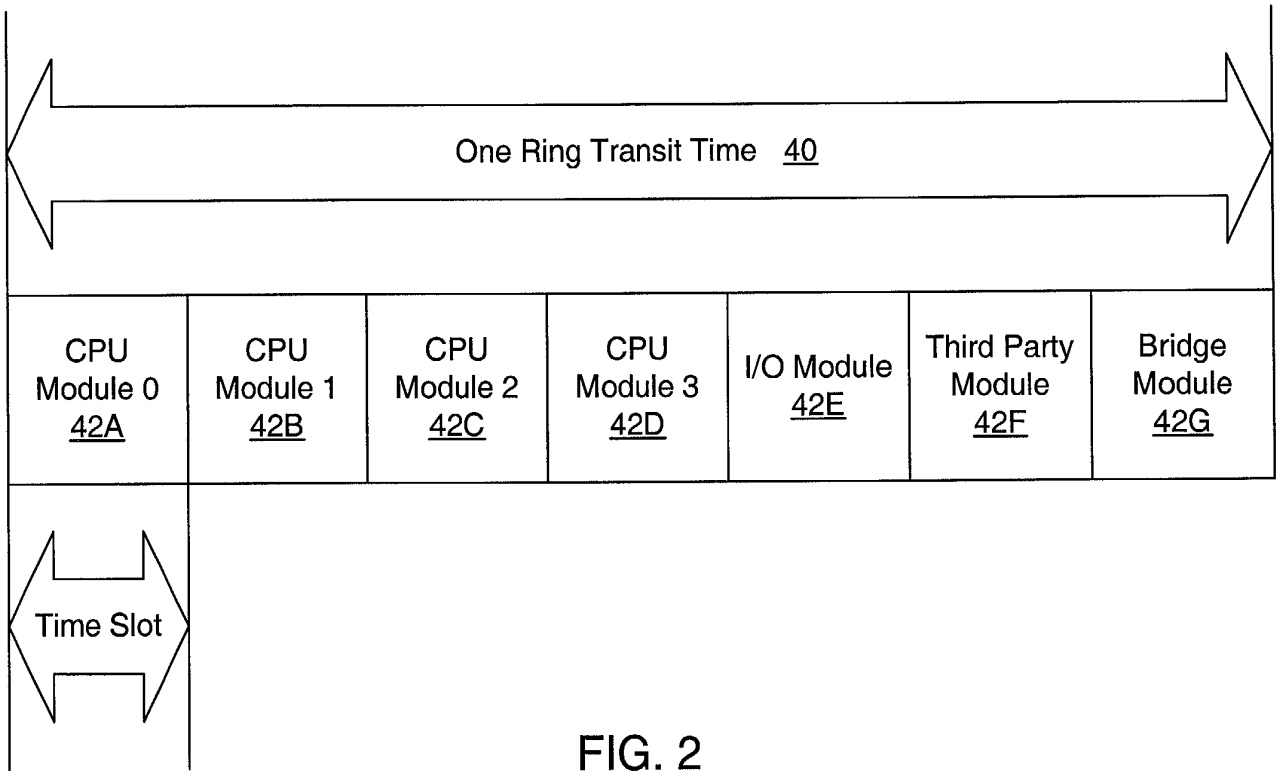
One Ring Transit Time 40
CPU Module 0 42A
CPU Module 1 42B
CPU Module 2 42C
CPU Module 3 42D
I/O Module 42E
Third Party Module 42F
Bridge Module 42G
Time Slot

FIG. 2

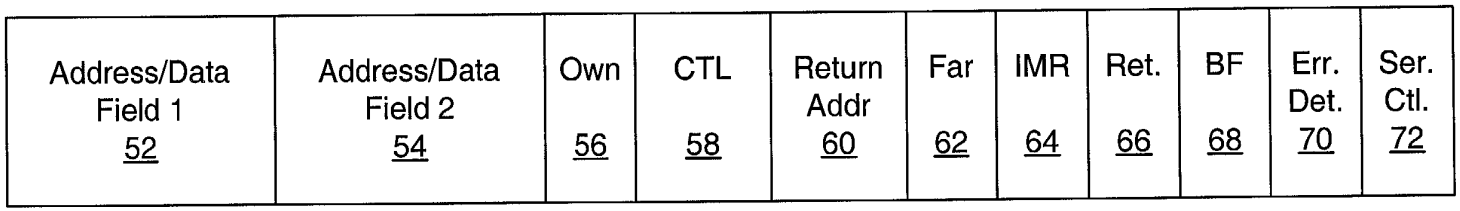
Address/Data Field 1 52
Address/Data Field 2 54
Own 56
CTL 58
Return Addr 60
Far 62
IMR 64
Ret. 66
BF 68
Err. Det. 70
Ser. Ctl. 72
50

FIG. 3

Operation Type	Address/Data Field 1	Address/Data Field 2
Read Near Request	Address 1	Address 2
Read Near Reply	Data 1	Data 2
Read Far Request	Address	Return Address
Read Far Reply	Return Address	Data
Write	Address	Data
Atomic Request	Address	Data
Atomic Reply	Address	Data
Read Chain - Frame 1	Address	Size and Return Address
Read Chain - Other Frames	Data	Data
Write Chain - Frame 1	Target Address	Source Address
Write Chain - Other Frames	Data	Data

82 84 86

86

FIG. 4

Control Field	Transaction
000	Null
001	Read
010	Write
011	Atomic
100	End Read Chain
101	Read Chain
110	Write Chain
111	End Write Chain

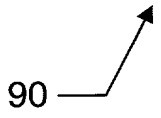

FIG. 5

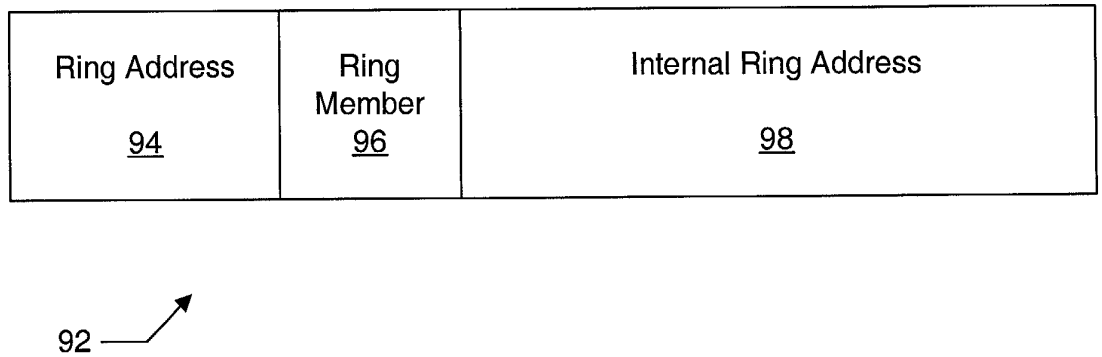

FIG. 6

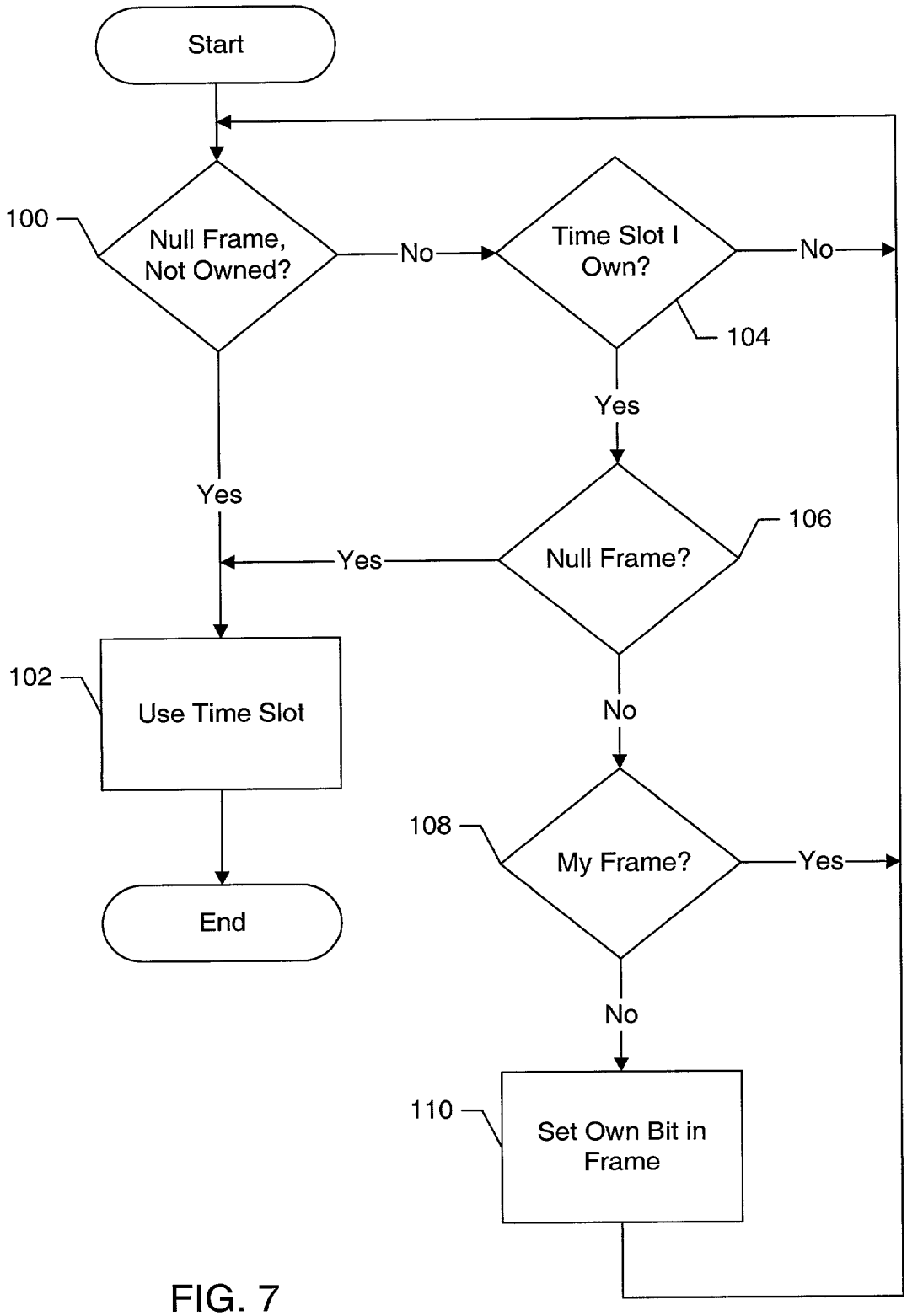
Start
100
Null Frame, Not Owned?
No
Time Slot I Own?
No
104
Yes
Yes
106
Null Frame?
Yes
102
Use Time Slot
No
108
My Frame?
Yes
End
No
110
Set Own Bit in Frame

FIG. 7

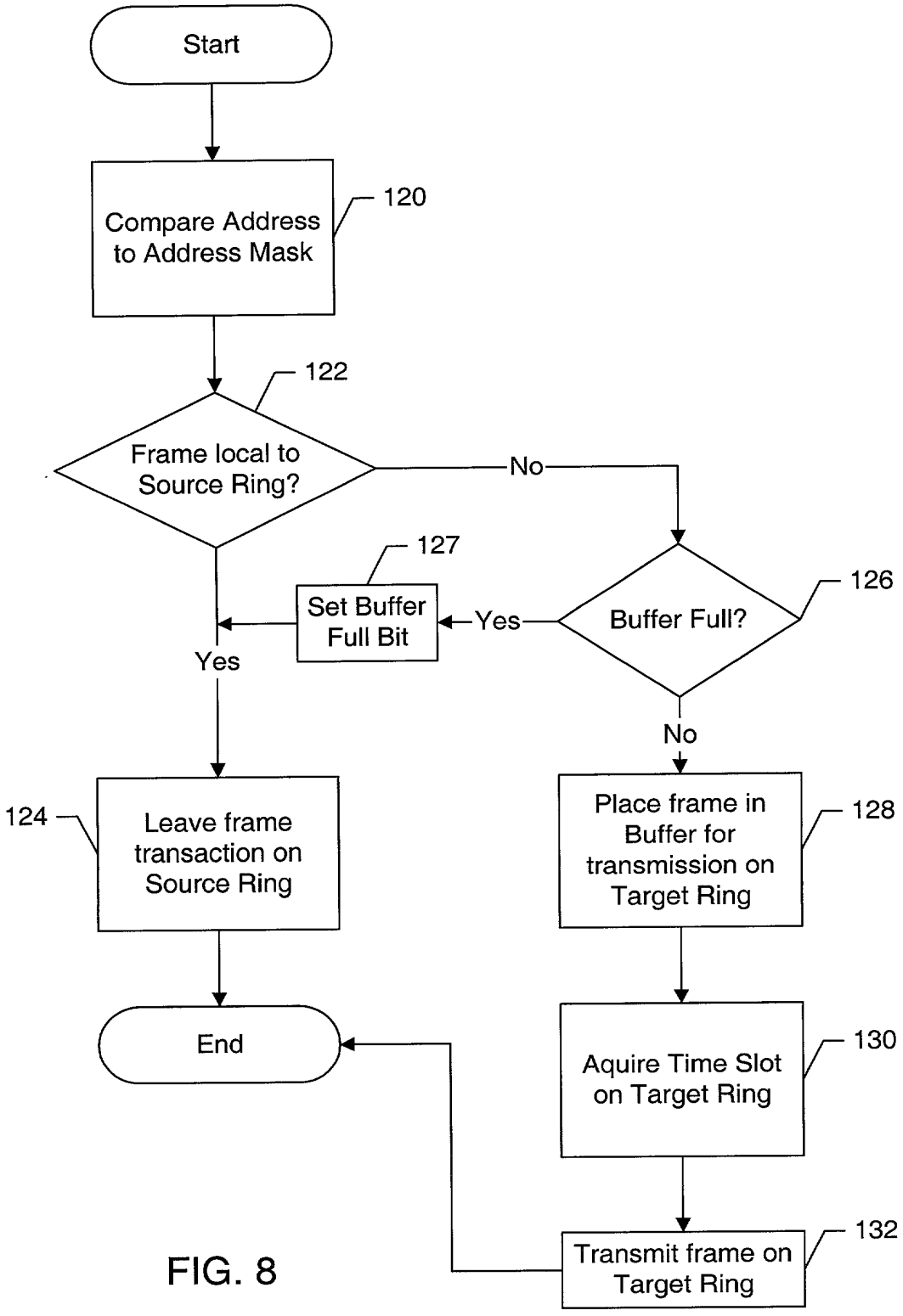
Start
Compare Address to Address Mask
120
122
Frame local to Source Ring?
No
Yes
127
Set Buffer Full Bit
Yes
Buffer Full?
126
No
124
Leave frame transaction on Source Ring
Place frame in Buffer for transmission on Target Ring
128
End
Aquire Time Slot on Target Ring
130
Transmit frame on Target Ring
132

FIG. 8

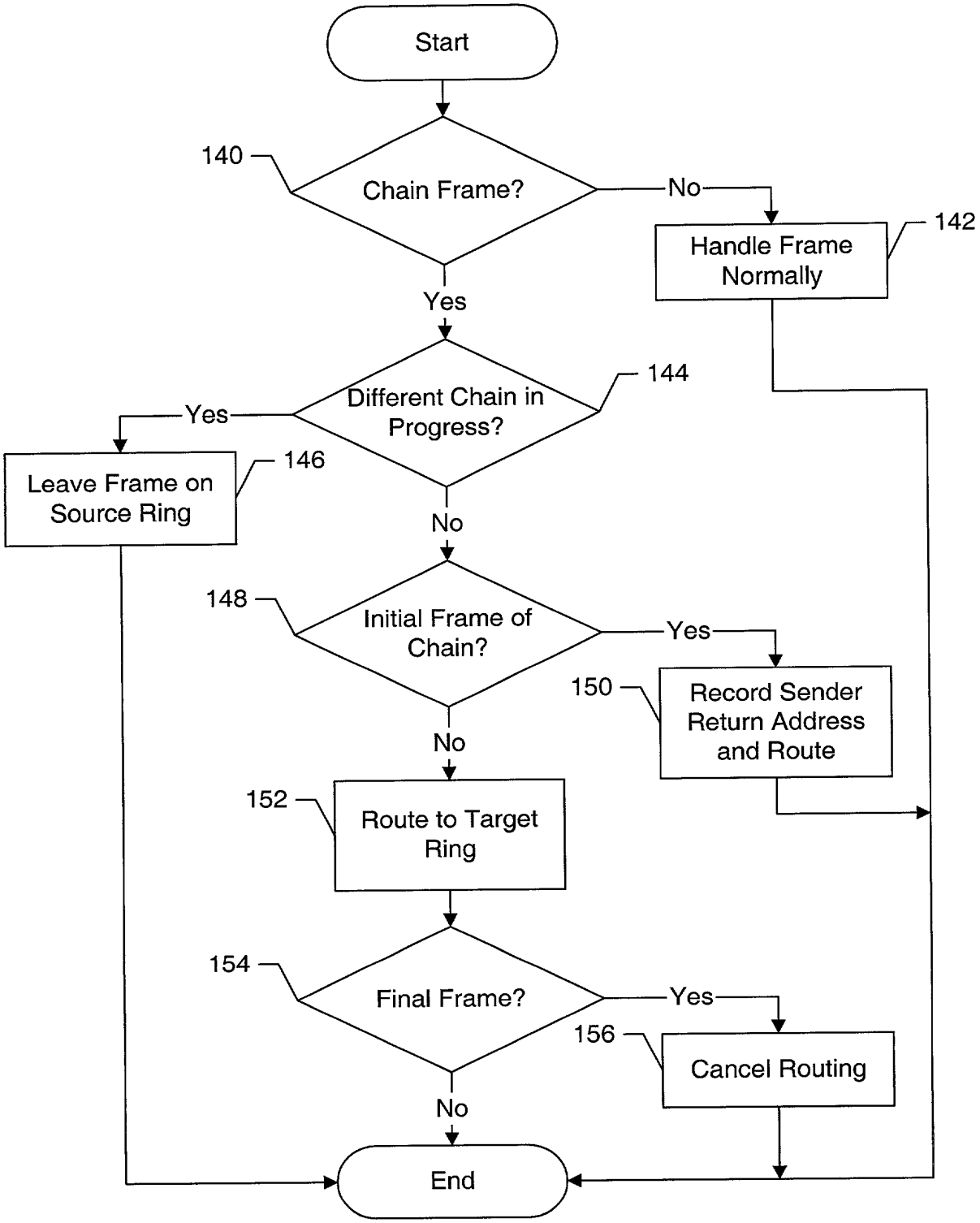
Start
140
Chain Frame?
No
142
Handle Frame Normally
Yes
144
Different Chain in Progress?
Yes
146
Leave Frame on Source Ring
No
148
Initial Frame of Chain?
Yes
150
Record Sender Return Address and Route
No
152
Route to Target Ring
154
Final Frame?
Yes
156
Cancel Routing
No
End

FIG. 9

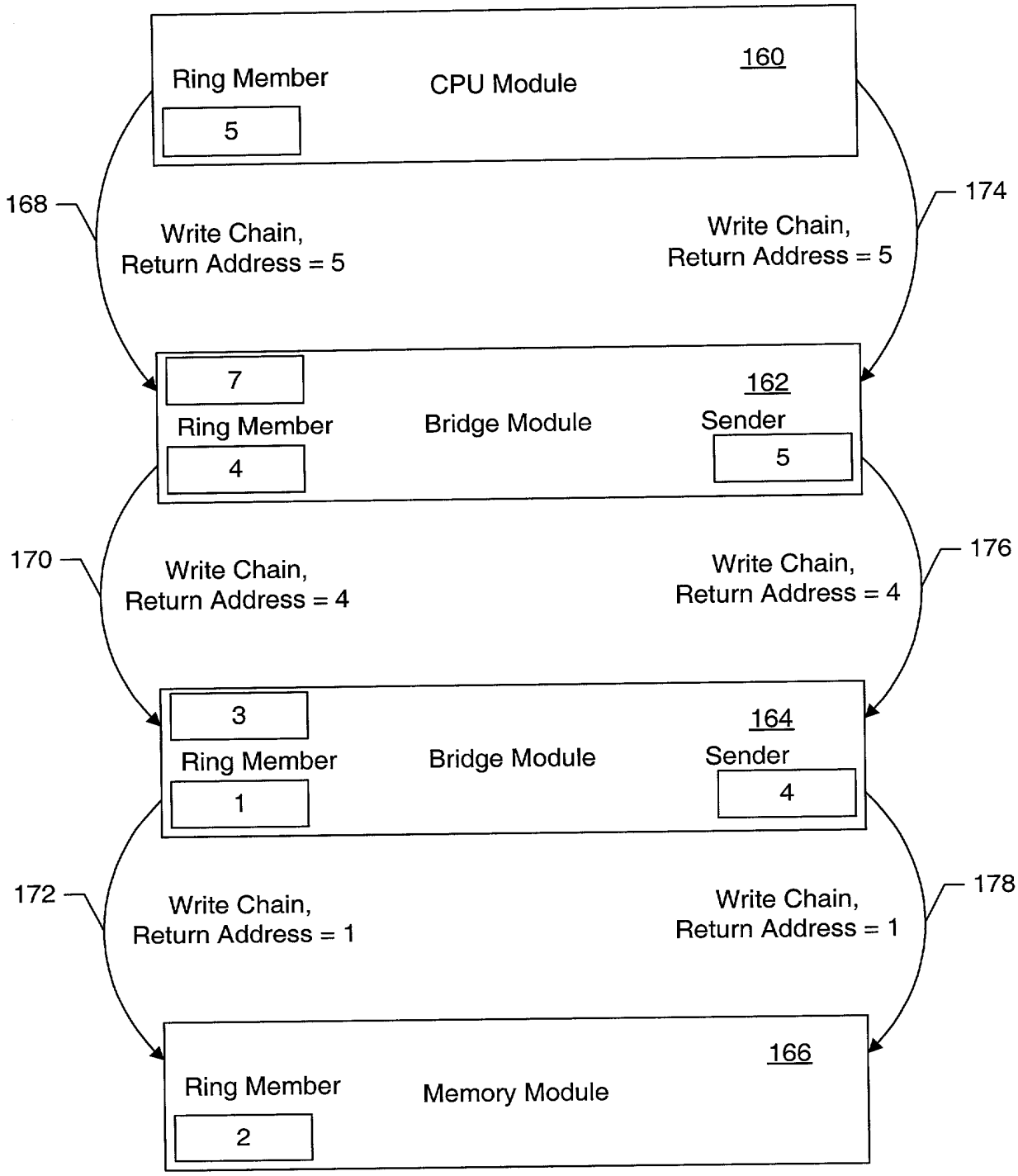
Ring Member
5
CPU Module
160
168
Write Chain,
Return Address = 5
Write Chain,
Return Address = 5
174
7
Ring Member
4
Bridge Module
162
Sender
5
170
Write Chain,
Return Address = 4
Write Chain,
Return Address = 4
176
3
Ring Member
1
Bridge Module
164
Sender
4
172
Write Chain,
Return Address = 1
Write Chain,
Return Address = 1
178
Ring Member
2
Memory Module
166

FIG. 10

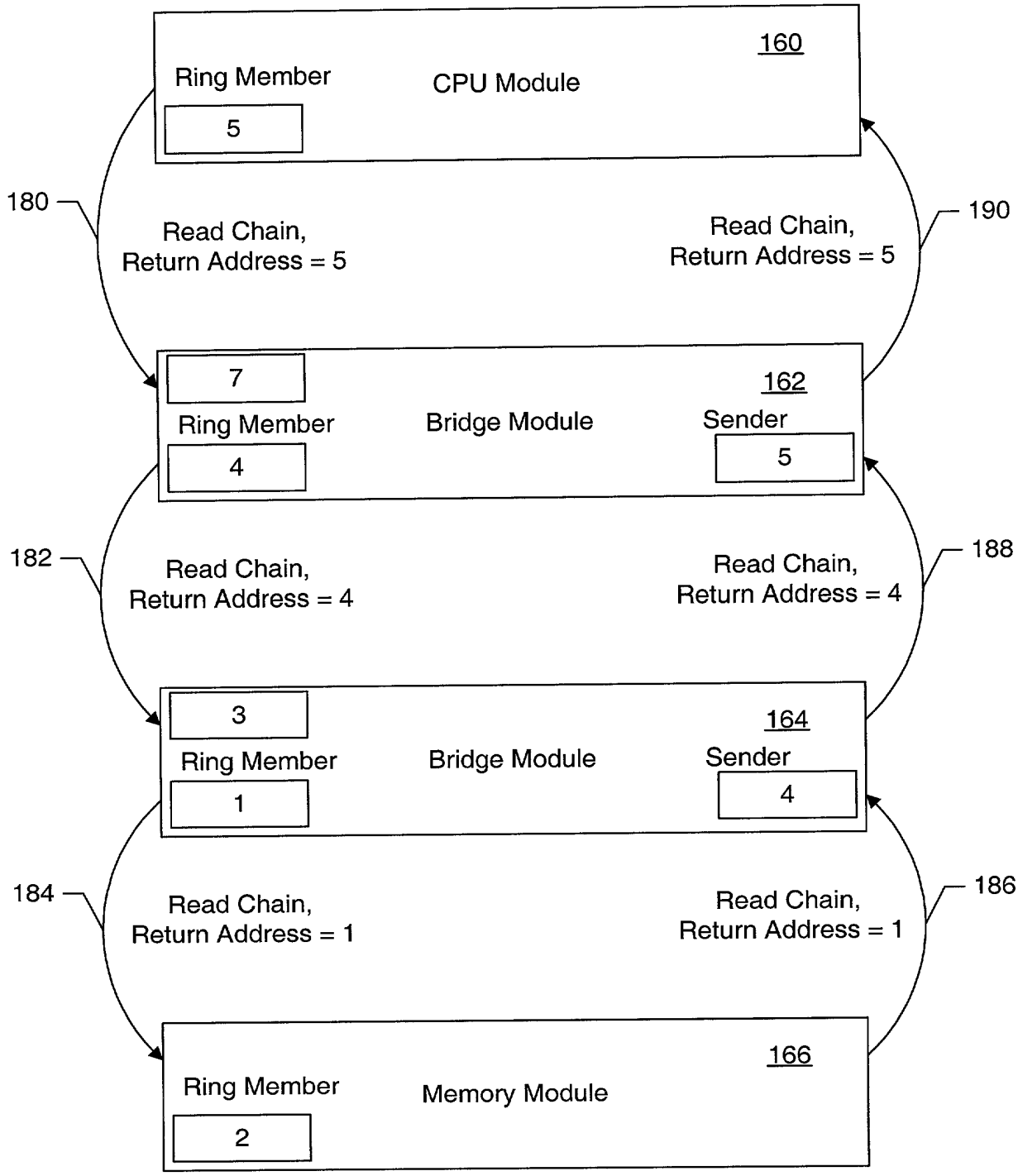
160
Ring Member
5
CPU Module
180
Read Chain,
Return Address = 5
190
Read Chain,
Return Address = 5
7
Ring Member
4
Bridge Module
162
Sender
5
182
Read Chain,
Return Address = 4
188
Read Chain,
Return Address = 4
3
Ring Member
1
Bridge Module
164
Sender
4
184
Read Chain,
Return Address = 1
186
Read Chain,
Return Address = 1
166
Ring Member
2
Memory Module

Fig. 11

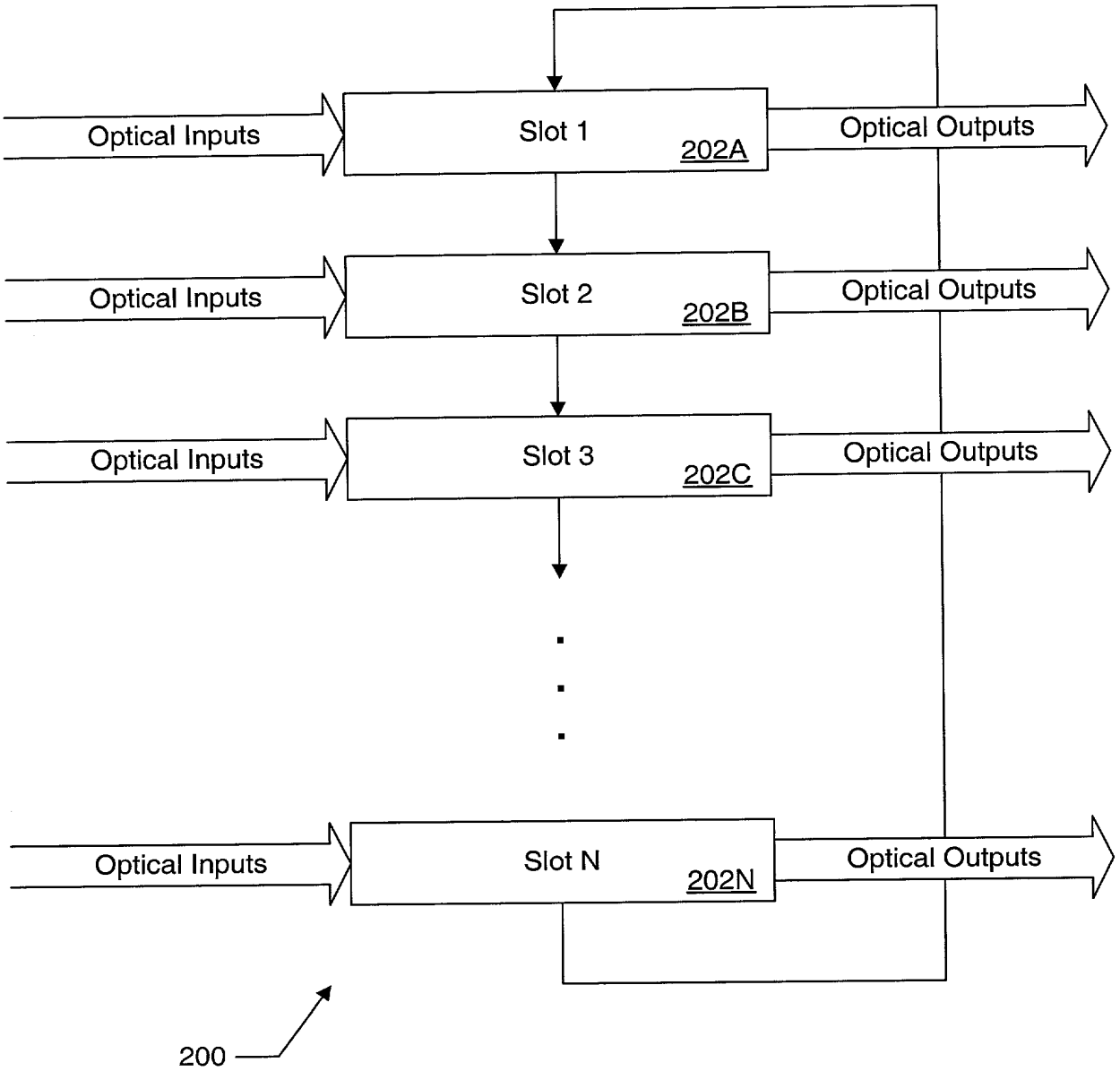
Optical Inputs
Slot 1
202A
Optical Outputs
Optical Inputs
Slot 2
202B
Optical Outputs
Optical Inputs
Slot 3
202C
Optical Outputs
Optical Inputs
Slot N
202N
Optical Outputs
200

FIG. 12